

FORM PTO-1449

INFORMATION DISCLOSURE STATEMENT

ATTY. DOCKET NO.
2210.0020002APPLICATION NO.
10/040,852FIRST NAMED INVENTOR
Tommy K. EngFILING DATE
December 28, 2001ART UNIT
2825

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
TD	AA1	6,360,356 B1	March 19, 2002	Eng			
	AB1						
	AC1						
	AD1						
	AE1						
	AF1						
	AG1						
	AH1						
	AI1						
	AJ1						
	AK1						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL1						Yes No
	AM1						Yes No
	AN1						Yes No
	AO1						Yes No
	AP1						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

TD	AR	1	Alcatel Telecommunications Review, 2nd Quarter, 1996, <u>The Challenge of Designing Million-Transistor ASICs</u> , H. Casier et al., pages 122-129
TD	AS	1	31st Design Automation Conference®, San Diego, CA, June 6-10, 1994, <u>Technology Mapping Using Fuzzy Logic</u> , Sasan Iman et al., pages 333-338
TD	AT	1	<u>Layout Driven Technology Mapping</u> , Massoud Pedram et al., 28th ACM/IEEE Design Automation Conference, pages 99-105

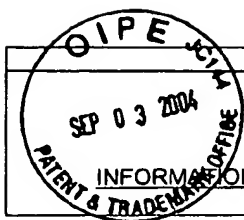
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DATE CONSIDERED

11-15-04

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.



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Page 2 of 2

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EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA2					
	AB2					
	AC2					
	AD2					
	AE2					
	AF2					
	AG2					
	AH2					
	AI2					
	AJ2					
	AK2					

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL2					Yes
	AM2					No
	AN2					Yes
	AO2					No
	AP2					Yes

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

TD	AR	2	Hewlett-Packard Journal, February 1995, Volume 46, Number 1, <u>Shortening the Time to Volume Production of High-Performance Standard Cell ASICs</u> , Jay D. McDougal et al., pages 91-96
TD	AS	2	<u>Layout-Driven RTL Binding Techniques for High-Level Synthesis</u> , Min Xu et al., 1996 IEEE, pages 33-38
TD	AT	2	Proceedings of the IEEE 1989 Custom Integrated Circuits Conference, May 15-18, 1989, <u>LOGOPT- A Multi-Level Logic Synthesis and Optimization System</u> , Ajit M. Prabhu, pages 4.1.1 - 4.1.4

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